WHAT IS CLAIMED IS:

1. A method of executing instructions in a microprocessor comprising:

fetching a conditional branch instruction from an instruction cache;

detecting branch prediction information in the branch instruction; and

responsive to the branch prediction information, fetching instructions from both a branch-taken path and from a branch-not-taken path of the branch instruction.

2. The method of claim 1, further comprising:

speculatively executing the instructions from the branch-taken path and the branch-not-taken path of the branch instruction;

executing the conditional branch instruction; and

based upon the outcome of the conditional branch instruction, discarding results from the speculatively executed instructions from the branch-taken path if the branch is not taken and discarding results from the branch-not-taken path if the branch is taken.

3. The method of claim 1, wherein the branch prediction information comprises compiler generated information indicative of the context in which the conditional branch instruction is used.

4. The method of claim 3, wherein the branch prediction information causes instruction fetching from both the taken and not taken branches if the branch instruction is determined by the compiler to be unpredictable.

5. The method of claim 1, wherein fetching instructions from the branch-taken path comprises fetching a predetermined number of instructions from the branch-taken path and wherein fetching instructions from the branch-not-taken path comprises fetching a predetermined number of instructions from the branch-not-taken path.

6. The method of claim 1, wherein fetching instructions from the branch-not-taken path comprises fetching instructions down the branch-not-taken path until a subsequent branch instruction is encountered.

7. A microprocessor comprising:

an instruction cache suitable for storing a set of processor executable instructions and configured to receive an instruction address and to retrieve an instruction corresponding to the instruction address; and

a fetch unit connected to the instruction cache and configured to generate an instruction address;

wherein the fetch unit is configured to detect branch instruction information in a branch instruction retrieved from the instruction cache and further configured to fetch instructions from both a branch-taken path and a branch-not-taken path of the branch instruction depending upon the state of the branch instruction information.

8. The microprocessor of claim 7, wherein the branch prediction unit includes prediction logic enabled by the branch instruction information and configured to predict the result of a branch instruction.

9. The microprocessor of claim 8, wherein the branch predicution unit includes a prediction bypass unit enabled by the branch prediction information and configured to issue instruction addresses from a branch-taken path and a branch-not-taken path of the branch instruction.

10. The microprocessor of claim 7 wherein the processor is configured to speculatively execute the instructions from the branch-taken path and from the branch-not-taken path of the branch instruction, execute the conditional branch instruction, and, based upon the outcome of the conditional branch instruction, discard results from the speculatively executed instructions from the branch-taken path if the branch is not taken and discarding results from the branch-not-taken path if the branch is taken.

11. The microprocessor of claim 7 configured to receive branch prediction information comprises compiler generated information indicative of the context in which the conditional branch instruction is used.

12. The microprocessor of claim 7, wherein the microprocessor is configured to fetch a predetermined number of instructions from the branch-taken path and further configured to fetch a predetermined number of instructions from the branch-not-taken path depending upon the state of the branch instruction information.

13. The microprocessor of claim 7, configured for fetching instructions down the branch-not-taken path until a subsequent branch instruction is encountered depending upon the state of the branch instruction information.

14. A data processing system including processor, memory, input means, and display, the processor including:

an instruction cache suitable for storing a set of processor executable instructions and configured to receive an instruction address and to retrieve an instruction corresponding to the instruction address; and

a fetch unit connected to the instruction cache and configured to generate an instruction address;

wherein the fetch unit is configured to detect branch instruction information in a branch instruction retrieved from the instruction cache and further configured to fetch instructions from both a branch-taken path and a branch-not-taken path of the branch instruction depending upon the state of the branch instruction information.

15. The microprocessor of claim 14, wherein the branch prediction unit includes prediction logic enabled by the branch instruction information and configured to predict the result of a branch instruction.

16. The microprocessor of claim 15, wherein the branch predicution unit includes a prediction bypass unit enabled by the branch prediction information and configured to issue instruction addresses from a branch-taken path and a branch-not-taken path of the branch instruction.

17. The microprocessor of claim 14 wherein the processor is configured to speculatively execute the instructions from the branch-taken path and from the branch-not-taken path of the branch instruction, execute the conditional branch instruction, and, based upon the outcome of the conditional branch instruction, discard results from the speculatively executed instructions from the branch-taken path if the branch is not taken and discarding results from the branch-not-taken path if the branch is taken.

18. The microprocessor of claim 14 configured to receive branch prediction information comprises compiler generated information indicative of the context in which the conditional branch instruction is used.

19. The microprocessor of claim 14, wherein the microprocessor is configured to fetch a predetermined number of instructions from the branch-taken path and further configured to fetch a predetermined number of instructions from the branch-not-taken path depending upon the state of the branch instruction information.